UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/922,300	09/02/1997	GEUN-WOO PARK	P54766	1404

7590 10/10/2003

ROBERT E BUSHNELL
ATTORNEY AT LAW
STE 300
1522 K ST NW
WASHINGTON, DC 200051202

EXAMINER	
MARC COLEMAN, MARTHE Y	

ART UNIT	PAPER NUMBER
3661	

DATE MAILED: 10/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

SN

Office Action Summary	Application No.	Applicant(s)	
	08/922,300	PARK, GEUN-WOO	
	Examiner	Art Unit	
	Marthe Y Marc-Coleman	3661	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to Applicant's response from the Board of Appeal decision on the rehearing dated 8/22/03.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art in view of Van Clifton Martin (U.S. Patent No. 3,555,348).

In regard to claims 1 and 4, Applicant discloses in the background of the invention:

- a pulse width modulation (PWM) controller for generating a PWM signal under the control of the microcomputer;
- a current amplifier for amplifying current in response to the PWM signal from the PWM controller;
- a horizontal/vertical(H/V) processor for driving a horizontal driver under the control of a microcomputer;
- the H/V processor outputs a horizontal pulse signal of square wave to the horizontal driver under the control of a microcomputer;

- a horizontal deflection coil is mounted to the next of a display device so that electron beams can be deflected to the left or right according to a direction of current flowing through the coil;
- an S-correction capacitor applies a parabola voltage to the horizontal deflection coil to correct a linearity of center-to-left and right sides of a screen of the display device;
- a horizontal output circuit for supplying current to a horizontal deflection coil and an S-correction capacitor in response to output signals from the current amplifier and horizontal driver;
- a horizontal/vertical (H/V) processor constant voltage circuit for supplying a constant voltage to the H/V processor to drive it;

Applicant admitted prior art does not disclose a power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

Van Clifton Martin discloses that the control grid 14 is clamped to a negative DC bias voltage –V1 from the power supply by a diode 44 connected between voltage-V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. **This diode-capacitor network makes the voltage at the control grid 14 drop slowly even though its bias voltage –V1 is removed** (see col. 2 lines 64-72).

As per the board rejection, Martin further discloses "a horizontal deflection yoke 17 and vertical deflection yoke 18 (see col. 2 line 19-21) Horizontal deflection control circuit 36 drives the beam off of the screen when protection is required, by producing additional current through the horizontal deflection yoke 17 (see col. 4 lines 40-44). In normal operation, the horizontal deflection of the beam is controlled by a signal from the horizontal or x-yoke drive 101 over line 55 at the base of NPN transistor 56. A second NPN transistor 58 at the base of NPN transistor 58 is normally off and is connected across transistor 56 with a current limiting resistor 549 connected therebetween. Transistor 58 is normally off and is connected across transistor 56 with a current limiting resistor 59 connected therebetween. Transistor 58 is normally off and current through transistor 56 controls a current through the horizontal deflection yoke 17. When it is necessary to protect screen 16, transistor 58 is turned on and additional current is drawn through the coil of the horizontal deflection yoke 17 so as to drive the beam off of the screen. The voltage for transistor 58 is from either of voltage sources +V4 and +V5. These two bias voltages are arranged so that if one fails the other will be present (see col. 1 lines 44-65). Martin further discloses (see col. 3 lines 65-69) that the value of these bias voltages are chosen so that even if the power supply fails, these voltages decay off at a slow enough rate so that transistor 58 will be turned on to cause the beam to be horizontally deflected off the screen".

At the time of the invention, it would have been obvious to one skilled in the art to utilize Van Clifton Martin's protection circuit with Applicant admitted prior art because it would protect the CRT display in case of sudden failures or malfunctions of circuits to the tube (see Van Clifton Martin col. 1 lines 36-39).

In regard to claim 3, Applicant admitted prior art discloses:

- a power supply circuit is adapted to convert commercial alternating current (AC) into direct current (DC) (see page 2 of the background of the invention lines 1-2);
- a horizontal deflection circuit under the control of a microcomputer, receiving said direct current input voltage, for horizontally deflecting electron beams generated in the cathode ray tube (see page 2 background of the invention lines 5-8)

Applicant admitted prior art does not disclose a power interruption delay charging means for gradually lowering said direct current input. In addition, Applicant's admitted prior art does not disclose a polarity capacitor and a diode connected to said polarity capacitor.

Van Clifton Martin discloses that the control grid 14 is clamped to a negative DC bias voltage –V1 from the power supply by a diode 44 connected between voltage-V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. **This diode-capacitor network makes the**

voltage at the control grid 14 drop slowly even thought its bias voltage –V1 is removed (see col. 2 lines 54-72).

As per the board rejection, Martin further discloses "a horizontal deflection yoke 17 and vertical deflection yoke 18 (see col. 2 line 19-21) Horizontal deflection control circuit 36 drives the beam off of the screen when protection is required, by producing additional current through the horizontal deflection yoke 17 (see col. 4 lines 40-44). In normal operation, the horizontal deflection of the beam is controlled by a signal from the horizontal or x-yoke drive 101 over line 55 at the base of NPN transistor 56. A second NPN transistor 58 at the base of NPN transistor 58 is normally off and is connected across transistor 56 with a current limiting resistor 549 connected therebetween. Transistor 58 is normally off and is connected across transistor 56 with a current limiting resistor 59 connected therebetween. Transistor 58 is normally off and current through transistor 56 controls a current through the horizontal deflection yoke 17. When it is necessary to protect screen 16, transistor 58 is turned on and additional current is drawn through the coil of the horizontal deflection yoke 17 so as to drive the beam off of the screen. The voltage for transistor 58 is from either of voltage sources +V4 and +V5. These two bias voltages are arranged so that if one fails the other will be present (see col. 1 lines 44-65). Martin further discloses (see col. 3 lines 65-69) that the value of these bias voltages are chosen so that even if the power supply fails, these voltages decay off at a slow enough

rate so that transistor 58 will be turned on to cause the beam to be horizontally deflected off the screen".

At the time of the invention, it would have been obvious to one skilled in the art to utilize Van Clifton Martin's protection circuit with Applicant admitted prior art because it would protect the CRT display in case of sudden failures or malfunctions of circuits to the tube (see Van Clifton Martin col. 1 lines 36-39).

In regard to claims 5 and 8, Applicant admitted prior art discloses in Fig. 2 and background of the invention:

- a pulse width modulation (PWM) controller for generating a PWM signal under the control of the microcomputer;
- a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;
- a current amplifier transformer having a primary coil and a secondary coil (see T1);
- a field effect transistor having its gate terminal connected to one terminal of said secondary coil (see FET1);
- one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller 135 through a capacitor and another terminal of said primary coil being connected to the ground terminal;

- said field effect transistor having a drain terminal connected to a high voltage source B+ and a source terminal connected in common to a second terminal of said secondary coil and one other side of a pulse transformer PT;
- said pulse transformer having a second side connected to one side of said horizontal deflection coil;
- a first diode connected between said source terminal and said drain terminal;
- a second diode connected between said second terminal of said secondary coil and said ground terminal;
- a H/V processor for generating a square wave pulse signal under the control of said microcomputer;
- a horizontal driver 144 for generating drive pulse signal in response to the square wave pulse signal from said H/V processor;
- an S-correction capacitor applies a parabola voltage to the horizontal deflection coil to correct a linearity of center-to-left and right sides of a screen of the display device;
- a horizontal output circuit for supplying current to a horizontal deflection coil and an S-correction capacitor in response to output signals from the current amplifier and horizontal driver;
- a horizontal/vertical (H/V) processor constant voltage circuit for supplying a constant voltage to the H/V processor to drive it;

Applicant admitted prior art does not disclose a power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

Van Clifton Martin discloses that the control grid 14 is clamped to a negative DC bias voltage –V1 from the power supply by a diode 44 connected between voltage-V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. **This diode-capacitor network makes the voltage at the control grid 14 drop slowly even thought its bias voltage –V1 is removed** (see col. 2 lines 64-72).

As per the board rejection, Martin further discloses "a horizontal deflection yoke 17 and vertical deflection yoke 18 (see col. 2 line 19-21) Horizontal deflection control circuit 36 drives the beam off of the screen when protection is required, by producing additional current through the horizontal deflection yoke 17 (see col. 4 lines 40-44). In normal operation, the horizontal deflection of the beam is controlled by a signal from the horizontal or x-yoke drive 101 over line 55 at the base of NPN transistor 56. A second NPN transistor 58 at the base of NPN transistor 58 is normally off and is connected across transistor 56 with a current limiting resistor 549 connected therebetween. Transistor 58 is normally off and is connected across transistor 56 with a current limiting resistor 59 connected therebetween. Transistor 58 is normally off and current through

transistor 56 controls a current through the horizontal deflection yoke 17. When it is necessary to protect screen 16, transistor 58 is turned on and additional current is drawn through the coil of the horizontal deflection yoke 17 so as to drive the beam off of the screen. The voltage for transistor 58 is from either of voltage sources +V4 and +V5. These two bias voltages are arranged so that if one fails the other will be present (see col. 1 lines 44-65). Martin further discloses (see col. 3 lines 65-69) that the value of these bias voltages are chosen so that even if the power supply fails, these voltages decay off at a slow enough rate so that transistor 58 will be turned on to cause the beam to be horizontally deflected off the screen".

At the time of the invention, it would have been obvious to one skilled in the art to utilize Van Clifton Martin's protection circuit with Applicant admitted prior art because it would protect the CRT display in case of sudden failures or malfunctions of circuits to the tube (see Van Clifton Martin col. 1 lines 36-39).

In regard to claims 2 and 9, Van Clifton Martin discloses:

- a polarity capacitor for performing charging operation and a diode connected to the polarity capacitor for preventing a voltage on the polarity capacitor from being discharged (see col. 2 lines 64-72 and Fig. 1 element 45);
- a diode connected to said polarity capacitor for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the

power supply to the display device is interrupted (see col. 2 lines 64-72 and Fig. 1 element 44).

In regard to claims 6 and 10, Applicant's admitted prior art discloses in Fig. 2 that said horizontal output circuit 234 comprises a horizontal output transistor TR having a collector terminal connected in common to said second side of said pulse transformer T2 and said one side of said horizontal deflection coil H-DY, an emitter terminal connected to said S-correction Capacitor Cs and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

In regard to claims 7 and 11, Applicant's admitted prior art discloses in Fig. 2:

- a second field effect transistor FET2 having a gate terminal connected to receive a square wave pulse signal from said horizontal/vertical processor 132, a source terminal connected to said ground terminal, and a drain terminal;
- a horizontal drive transformer T2 having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source V2 through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and
- said secondary coil of said horizontal drive transformer T2 having one side connected to said base terminal or said horizontal output transistor 134 and a second side connected to said ground terminal.

Response to Arguments

4. Applicant's arguments filed on 8/22/03 have been fully considered but they are not persuasive.

Applicant argues the following:

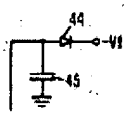
- it is not obvious to combine Applicant admitted prior art with Van Clifton Martin;
- Martin fails to teach or suggest, to one of ordinary skill in the art, gradually lowering the input voltage to a H/V processor constant voltage circuit when power supplied to the display device is interrupted.

Examiner disagrees with the applicant argument:

In regard to claims 1, 3, and 8, Applicant concedes that Applicant's admitted prior art (see Fig. 2; and Description of related art in the Background of the Invention) teaches all that is claimed except the feature of power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

Martin's discloses a protection circuit for a display device which ensures screen protection in case of sudden failures or malfunctions of circuits to the tube (see col. 1 lines 35-39), which ensures that the screen will not be damaged by a strong beam current (see col. 1 lines 5-8). Martin specifically discloses : **" This diode-capacitor network makes the voltage at the control grid 14 drop slowly even thought its bias voltage –V1 is removed"** in col. 2 lines 63-72.

In other words not only does Martin teach the structure, the functionality of the circuit arrangement, Martin also applies the above circuit configuration to gradually or slowly lower the DC input voltage as claimed by applicant.

By incorporating Martin's power interruption delay charging circuit as depicted in Martin's Fig. 1, a portion of which is adjoined herein 

(which is a well known circuitry) including a voltage prevention diode 44, a capacitor 45, a bias voltage, into the prior art admitted by the Applicant in Fig. 2 one of the ordinary skill in the art can easily comes up with the Applicant's invention.

In order words Martin has the same structure as the claimed circuitry. It is seen that Martin's circuitry performs the same function as the circuitry claimed by applicant.

According to the Board of Appeal, "from the disclosure of Martin that voltages +V4 and +V5 will decay off at a slow enough rate so that transistor 58 will be turned on to cause the beam to be deflected off of the screen if the power supply fails, it is clearly seen that Martin teaches gradually lowering the input voltages +V4 and +V5 to the deflection yoke when the power supply to the display device is interrupted".

It is therefore obvious that one of the ordinary skill in the art would be motivated to use the technique of a power interruption delay charging structure to lower voltages applied slowly in order to protect display apparatus from harmful effects such as power surges, electrical spikes, high beam currents, etc. Therefore, one can

clearly see that the approach of gradually decreasing voltages is well known, thereby rendering applicant's claimed invention obvious, hence unpatentable.

With respect with the argument that " Martin's teaching fails to suggest modification of the Applicant admitted prior art (AAPA) by **gradually lowering an input voltage to the horizontal/vertical processor constant voltage circuit** 131 of the AAPA and the Board has failed to provide a *prima facie* basis of support for suggesting that such a modification would have been obvious.

Examiner agrees with the Board decision "as long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventor. See in re Dillon, 919 F.2d 688, 693, 16 USPQ 2d 1897, 1901 (Fed. Cir. 1990) (en banc), Cert. Denied, 500 US 904 (1991) AND In re BEATTIE, 974 F.2d 1309, 1312, 24 USPQ2d 1040, 1041 (Fed. Cir. 1992).

In response to the Applicant's arguments concerning the Board of Appeal rejection, the Examiner has mentioned new portions of the art reference that the Board of Appeal has mentioned, and were not used in the prior final office action. This does not constitute a new ground of rejection. It is clear that the prior art reference is of record and has been considered entirely by Applicant. See In re Boyer, 3653F.2d 455, 458n.2, 150 USPQ 441, 444, N.2(CCPA1966) and In re Bush, 296F.2d 491, 131 USPQ 263 267 (CCPA 1961).

The mere fact that additional portions of the same reference may have been mentioned or relied upon does not constitute new ground of rejection. In re Meinhardt, 392 F.2d 273, 280, 157 USPQ 270, 275 (CCPA1968).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marthe Y Marc-Coleman whose telephone number is (703) 305-4970. The examiner can normally be reached on Monday-Thursday from 9:30 AM - 8:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William A Cuchlinski can be reached on (703) 308-3873. The fax phone

number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1113.

Patent Examiner
Marthe Y. Marc-Coleman
Marthe Marc-Coleman

October 7, 2003